PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : B01L 7/00

A1

(11) International Publication Number: WO 00/32312

(43) International Publication Date: 8 June 2000 (08.06.00)

(21) International Application Number: PCT/GB99/03994

(22) International Filing Date: 30 November 1999 (30.11.99)

(30) Priority Data:
9826237.1 30 November 1998 (30.11.98) GB

(71) Applicant: HYBAID LIMITED [GB/GB]; Action Court, Ashford Road, Ashford, Middlesex TW15 1XB (GB).

(72) Inventor: FRIPP, David; Hybaid Limited, Action Court, Ashford Road, Ashford, Middlesex TW15 1XB (GB).

(74) Agents: JEHAN, Robert et al.; Williams, Powell & Associates, 4 St. Paul's Churchyard, London EC4M 8AY (GB).

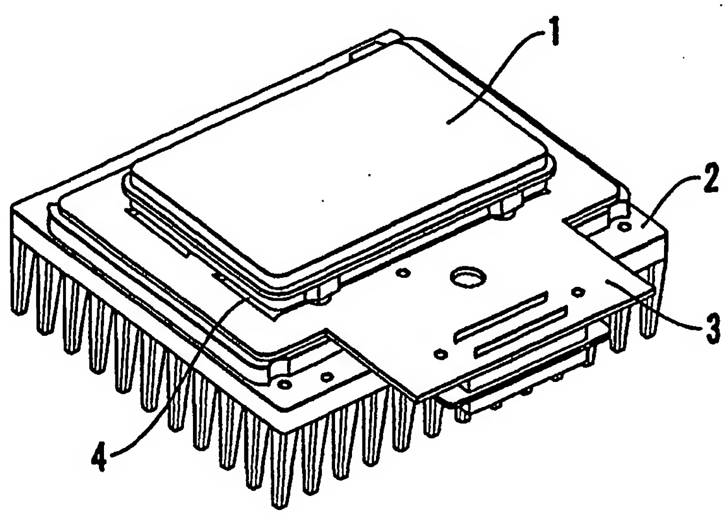
(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: THERMAL CYCLER

(57) Abstract

A thermal cycler for controlled heating and cooling of biological samples uses eight Thermoelectric Coolers (TECs), positioned between a metal sample plate and a heat sink (2). By altering the polarity of the applied current through the TEC, the temperature of the sample plate can be raised or lowered. When uniform heating and cooling of the sample plate is required, all eight TECs are connected in series and in the same polarity. To produce temperature gradients accross the sample plate, the relative polarity of individual TECs is changed or they are bypassed altogether.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

THERMAL CYCLER

The present invention relates to a thermal cycler for use in carrying out controlled heating and cooling of biological samples, for example DNA strands.

Traditionally, scientists have used the technique of the Polymerase Chain Reaction (PCR) to synthesise defined sequences of DNA. This generally involves a three step procedure: separation of the DNA to be amplified (template DNA); annealing of short complimentary DNA sequences (primers) to the template DNA and finally the addition of deoxynucleotides to the primer strands in order to copy the template DNA. This is usually performed in a thermal cycling machine where a cycle of three different temperatures is repeated approximately 25-35 times. Template DNA separation and synthesis steps occur at defined temperatures. However, the temperature at which the primer binds to the DNA, may need optimising in order for this step to occur efficiently and achieve desirable PCR results. Primer annealing optimisation experiments usually involve setting up a number of different experiments where only the primer annealing temperature is varied. The experiment may need to be performed 3 or 4 times in order to determine the optimum binding temperature. These experiments would have to be repeated each time a new set of primers was required for different PCRs. The development of a temperature gradient block enables the scientists to determine the optimum binding temperatures of several primer sets in a single experiment.

However, prior art derives which produce a thermal gradient have been relatively complex and expensive.

The present invention seeks to provide an improved thermal cycler.

According to an aspect of the present invention, there is provided a thermal cycler including a sample plate able to

hold a plurality of samples, a plurality of heating and cooling elements located along the sampling plate, supply means operable to provide a current to the heating and cooling elements, and switching means able to switch current individually through each heating or cooling element or each of a plurality of sets of heating or cooling elements.

The temperature gradient block can achieve a set of discrete temperatures simultaneously, thereby decreasing the number of optimisation experiments the scientist needs to perform and therefore the workload.

An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a perspective view of an embodiment of heating and cooling block of a thermal cycler;

Figure 2 shows different elevational views of the block of Figure 1 with the sample plate attached and removed to reveal a plurality of heating and cooling elements;

Figures 3 to 8 show an example of circuit diagram for driving the heating and cooling elements of Figure 2 in different manners; and

Figure 9 is a graph showing the time/temperature characteristics of the thermal cycler of Figure 1.

Controlled heating and cooling of biological samples is preferably achieved by using Thermoelectric Coolers (TECs). This embodiment uses 8 such devices, positioned between a metal sample plate and a heat sink 2 arranged a shown in Figure 1.

A TEC will generate a temperature differential across its surfaces when a current is applied. By altering the polarity of the applied current, the temperature of the sample plate can be raised or lowered, as is known in the art. When uniform heating and cooling of the sample plate is required, all 8 TECs are connected in series and in the same polarity. To produce temperature gradients across the sample plate, the relative polarity of individual TECs is changed or they are bypassed altogether.

Referring to Figure 2, a circuit board 3 (described in greater detail below) is located on the heat sink, and in this example, eight TECs 4 are located over the circuit board 3. The sample plate 1 is of conventional form and typically is able to hold many samples in an organised array.

Referring to Figures 3 to 8, the circuit used to deliver current to the TECs 4 is shown in various operating states. The specific component types mentioned below are given by way of example only. The skilled person will readily be able to find alternatives.

Current flow through the TECs is switched by means of MOSFETs (International Rectifier IRLI3705N) shown in Figure 3 as Q1-Q6. The design uses International Rectifier PVI5100 Photovoltaic Isolators, U1-U6, to provide a gate drive voltage for each MOSFET which is isolated from the control interface.

To achieve uniform heating and cooling, control signal C2 is set to logic "1" to provide base current for Q12 which activates U3 and U5 and enables MOSFETs Q1 and Q4. With a positive voltage on A with respect to B, current flow in the TECs is as shown in Figure 4, resulting in uniform cooling of the sample plate 1. With a negative voltage on A with respect to B, current flow in the TECs is as shown in Figure 5, resulting in uniform heating of the sample plate. In this

case, current flows through the parasitic diodes in Q1 and Q4.

To achieve a temperature gradient across the sample plate 1, control signal C1 is set to logic `1' to provide base current for Q7 which activates U2 and U1 and enables MOSFETs Q2 and Q6. With a positive voltage on A with respect to B, current flow in each of the TECs is as shown in Figure 6, resulting in a cooling effect in TECs P1, P2, P3 and P4 and a heating effect in TECs P5, P6, P7 and P8. Note that in this case, current flows through the parasitic diode in Q3.

In order to obtain a more linear gradient across the sample plate 1, less heating/cooling is required from the inner TECs P3, P4, P5 and P6. This is achieved by bypassing these TECs whilst keeping TECs P1, P2, P7, and P8 in a `gradient' configuration. Control signals C1 and C0 are set to logic `1' to provide base current for Q7 and Q13 which activates U1, U2, U4 and U6, and enables MOSFETs Q2, Q3, Q5 and Q6. With a positive voltage on A with respect to B, current flow in the TECs is as shown in Figure 7, resulting in a cooling effect in TECs P1 and P2 and a heating effect in TECs P7 and P8. Note that in this case current flows through the parasitic diode in Q3.

By setting control signals C2 and C0 to logic `1' base current is provided for Q12 and Q13 which activates U3, U4, U5 and U6 and enables MOSFETs Q1, Q3, Q4 and Q5. With a negative voltage on A with respect to B, current flow in the TECs as shown in Figure 8, resulting in a heating effect in TECs P1, P2, P3 and P4 only. This mode of operation is used to help re-establish temperature uniformity across the sample plate. Note that in this case current flows through the parasitic diode in Q2.

It will be apparent that the current through the inner TECs P3, P4, P7 and P8 can be switched intermittently to produce

any desired temperature gradient, as can be done with the outer TECs P1, P2, P5 and P6. The duty cycles suitable for the various TECs can be determined by experimentation.

Figure 9 shows a typical temperature/time characteristic obtained using this technique. Each line on the graph represents the temperature of particular locations on a line running from left to right across the sample plate 1.

Zone A represents uniform cooling or heating. Current flow through the TECs is as shown in Figure 4 (cooling) and Figure 5 (heating).

Zone B represents operation in gradient mode. In this mode, uniform heating and cooling is used in combination with the gradient operation, represented in Figure 6 and 7, to achieve the desired temperature set-point and the desired temperature gradient.

Zone C represents the recovery from gradient mode. Temperature uniformity across the sample plate is re-established by a combination of uniform heating and partial heating represented in Figure 8.

It will be apparent that the pairing of TECs for the purposes of heating/cooling is merely exemplary.

A description of the preferred method of operation of the system, advantageously provided in software, is given below.

The eight Peltier Thermo Electric Coolers (TECs) are wired in four pairs of two. Three control signals are used to switch the arrangement of Field Effect Transistors (FETs) Q1 to Q4, which in turn are used to switch pairs of TECs in or out of the circuit. The four pairs of TECs can be driven in the following modes:

1. Common mode, where all four pairs are used for heating or cooling.
2. Differential mode, where two pairs at one end are used for heating and two pairs at the opposite end are used for cooling. This mode is used during a gradient step.
3. Half Differential mode, where the two outer pairs only are driven. This mode is used to improve linearity across the block during a gradient step.
4. Start Gradient mode, where the two pairs used at the cooler end of the block are cooled, and the other two pairs are not driven. This mode is used when starting a gradient step.
5. Stop Gradient mode, where the two pairs at the cooler end of the block are heated, and the other two pairs are not driven. This mode is used when ending a gradient step.

A PID loop controls the temperature of the block, based on measurements taken from a thermistor embedded in one end of the block. Switching the TECs between the various operating modes for a calculated period of time enables the temperature gradient to be accurately controlled.

FET States

The Gradient Temperature Block circuitry gives nine possible FET states. These states are the combination on the three control bits C2, C1 and C0, with the power supply polarity, + or -.

Each of the sixteen combinations are named 0+, 0-, 1+, 1- .... 7+, 7-.

Of these sixteen combinations, only nine are usable because the FETs have diodes allowing reverse current to flow:

NAME	1 2 3 4	STATES
Off	- - - -	0-, 1-
Heat	H H H H	0+, 2+, **4+**, 6+
Cool	C C C C	**4-**
Differential	C C H H	**2-**
Start Gradient	C C - -	**6-**
Stop Gradient	H H - -	1+, 3+, **5+**, 7+
Half Differential	C - - H	**3-**
Cool Ends	C - - C	5-
Not Used (!)	C c h c	7-

Column 1 represents the variable (cooler) end of the block, column 4 is the fixed end.

H indicates Heating, C is Cooling and - is no change

Mode 7- is not used because it gives c=1/3 Cooling and h=1/3 Heating

Only the states in **bold** are used in the Express program

State 6- is only on for one time slot, and has a negligible effect. It is thought that this method of starting up a gradient was never fully implemented.

A 50:50 ratio mix of 2- and 3- gives an average as follows:

2-	C	C	H	H
3-	C	-	-	H
Sum	2C	C	H	2H

This gives a linear slope

State 3+ indicates the C2=0, C1=C0=1 and the power supply is in Positive mode.

This corresponds to the +ve supply connected to the B terminal on the circuit diagram.

Mode of Operation

A global variable called gradient is set when the temperature gradient needs to be changed. This is calculated from the measured gradient and required gradient.

In Normal mode *CurrentDemand(0)* is used to set the power supply.

In Gradient mode *CurrentDemand(1)* is used to set the power supply. This is clipped to 0 or negative values since the Differential, Half Gradient and Reverse Differential FET states only work with one direction of current.

In Normal modes, one time value, *called ZoneTime(0)*, is calculated from the *CurrentDemand(0)* value.

In Gradient modes, two time values are calculated from the *CurrentDemand(1)* value. These are called *ZoneTime(0)* and *ZoneTime(1)*.
ZoneTime(1) is always set to one half of *ZoneTime(0)*.
ZoneTime(0) is the number of time slots out of 190 which the power supply is on.
ZoneTime(1) marks the mid point of *ZoneTime(0)* so that in increasing gradient mode the FET state can be 50% differential and 50% half differential (ends only).

A finite sate machine called *UpdateCurrentDemand* is used to control the process-

State 0 initialises variables

State 1 decides on one of three sub-machines:

1. Normal

2. Increase the gradient
3. Decrease the gradient

For an increase or decrease in gradient 256/446 slots are Normal mode and 190 are Gradient mode.

Normal Mode:

The process is divided up into 190 timeslots.
The FET state is switched to Normal.
The power supply is on for *ZoneTime(0)* out 190 slots, then switched off.

Increasing Gradient Mode:

The process is divided up into 190+256=446 timeslots.
The FET state is Differential(2-) for half *ZoneTime(0)*, then Half Differential(3-) for another half *ZoneTime(0)*. (This gives a more linear slope than just one of the states on its own).
Then the power supply is switched off until slot 191.
Then the FET state is switched to Normal (4+, 4-) and Gradient mode disabled for 258 slots.

Decreasing Gradient Mode:

The process is divided up into 190=266=446 timeslots.
The FET state is Reverse Differential(5+) for *ZoneTime(0)*.
The FET state is then switched to Normal and Gradient mode disabled for 256 slots.
Then the power supply is switched off until slot 191.
Then the FET state is switched to Normal (4+, 4-) and Gradient mode disabled for 256 slots.

For either gradient mode the power supply is on for *ZoneTime(0)* in gradient mode (if required) out of the first 190 slots, then for another *ZoneTime(0)* out of the next 256 slots in normal mode.

Summary

In normal (non gradient) mode the power supply is pulse width modulated so that it is on for *ZoneTime(0)* slots out of 190. The PWM ratio is calculated by the main PID loop.

In gradient mode, when a change of gradient is required, the FET state is adjusted to give the required change, and the gradient PID loop calculates the *ZoneTime(0)*, *ZoneTime(1)* and required current.

When the 190 slots are completed, the unit is switched into normal mode for 256 slots, so that the overall block temperature can be adjusted. If a change in gradient is not required the unit remains in normal mode.

The disclosures in British patent application no. 9826237.1, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

CLAIMS

1. A thermal cycler including a sample plate able to hold a plurality of samples, a plurality of heating and cooling elements located along the sampling plate, supply means operable to provide a current to the heating and cooling elements, and switching means able to switch current individually through each heating or cooling element or each of a plurality of sets of heating or cooling elements.

2. A thermal cycler according to claim 1, wherein the switching means is operable selectively to switch the direction of current through the heating and cooling elements.

3. A thermal cycler according to claim 1 or 2, wherein the switching means is operable selectively to disconnect the supply means from the heating and cooling elements.

4. A thermal cycler according to claim 1, 2 or 3, wherein the switching means is operable to connect at least some of the heating and cooling elements in series with one another.

5. A thermal cycler according to any preceding claim, wherein the switching means is operable to switch the supply to provide current in a first direction to some of the heating and cooling elements and in a second direction to others of the heating and cooling elements.

6. A thermal cycler according to any preceding claim, wherein the switching means is operable to switch the supply to provide current intermittently to one or more of the heating and cooling elements.

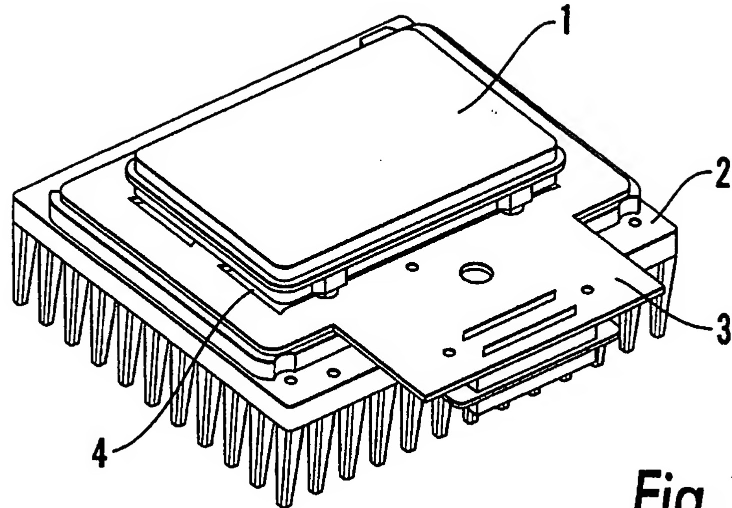


Fig. 1

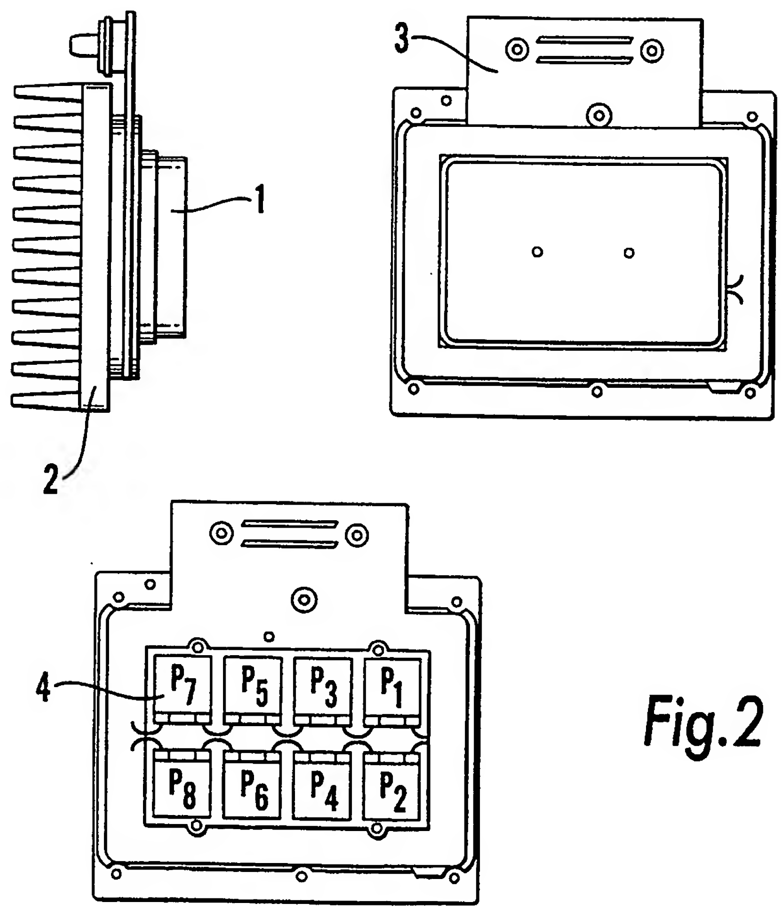


Fig. 2

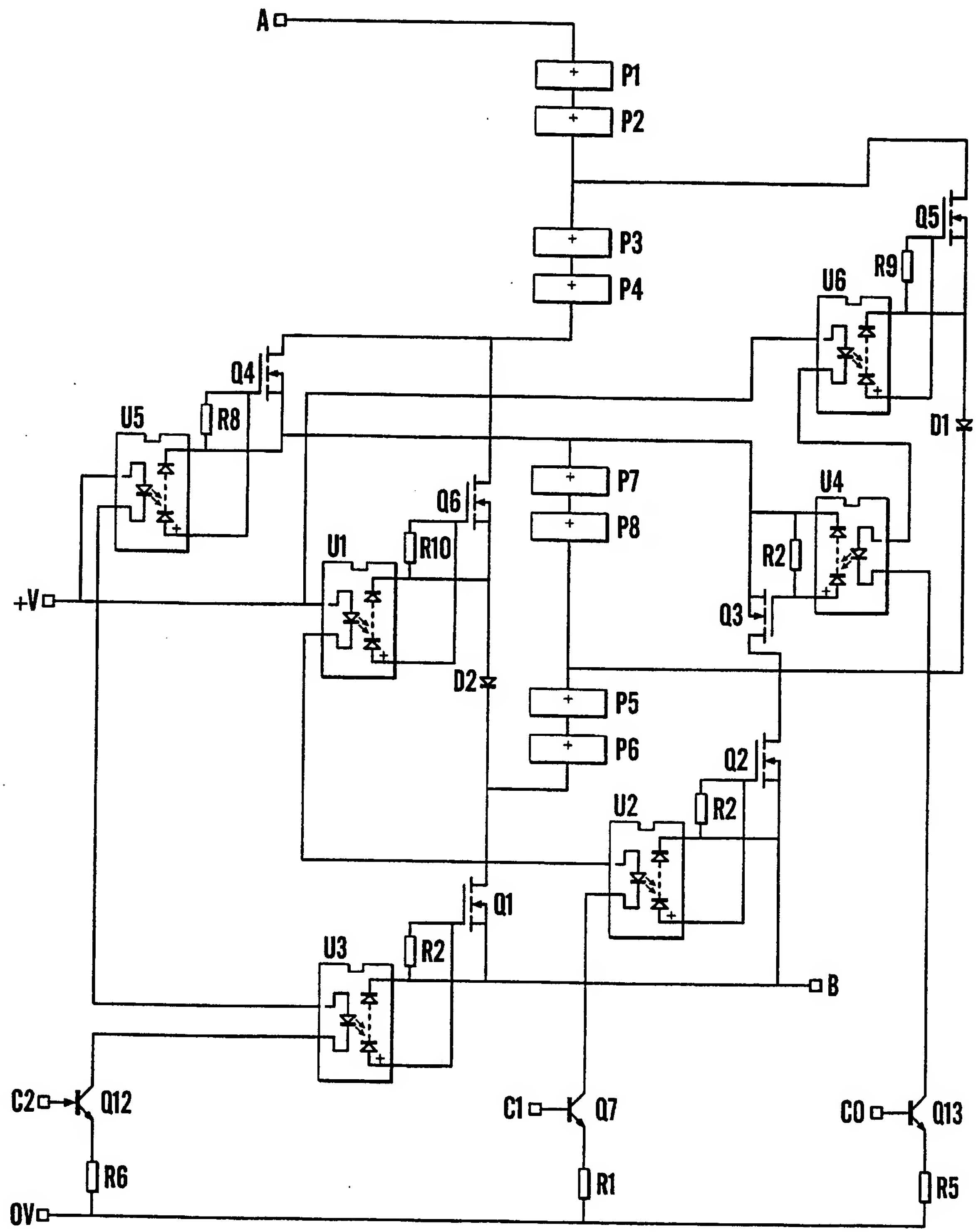

A
P1
P2
P3
P4
Q5
R9
U6
Q4
U5
R8
D1
P7
P8
U4
Q6
R10
U1
R2
+V
Q3
D2
P5
P6
Q2
U2
R2
Q1
U3
R2
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.3

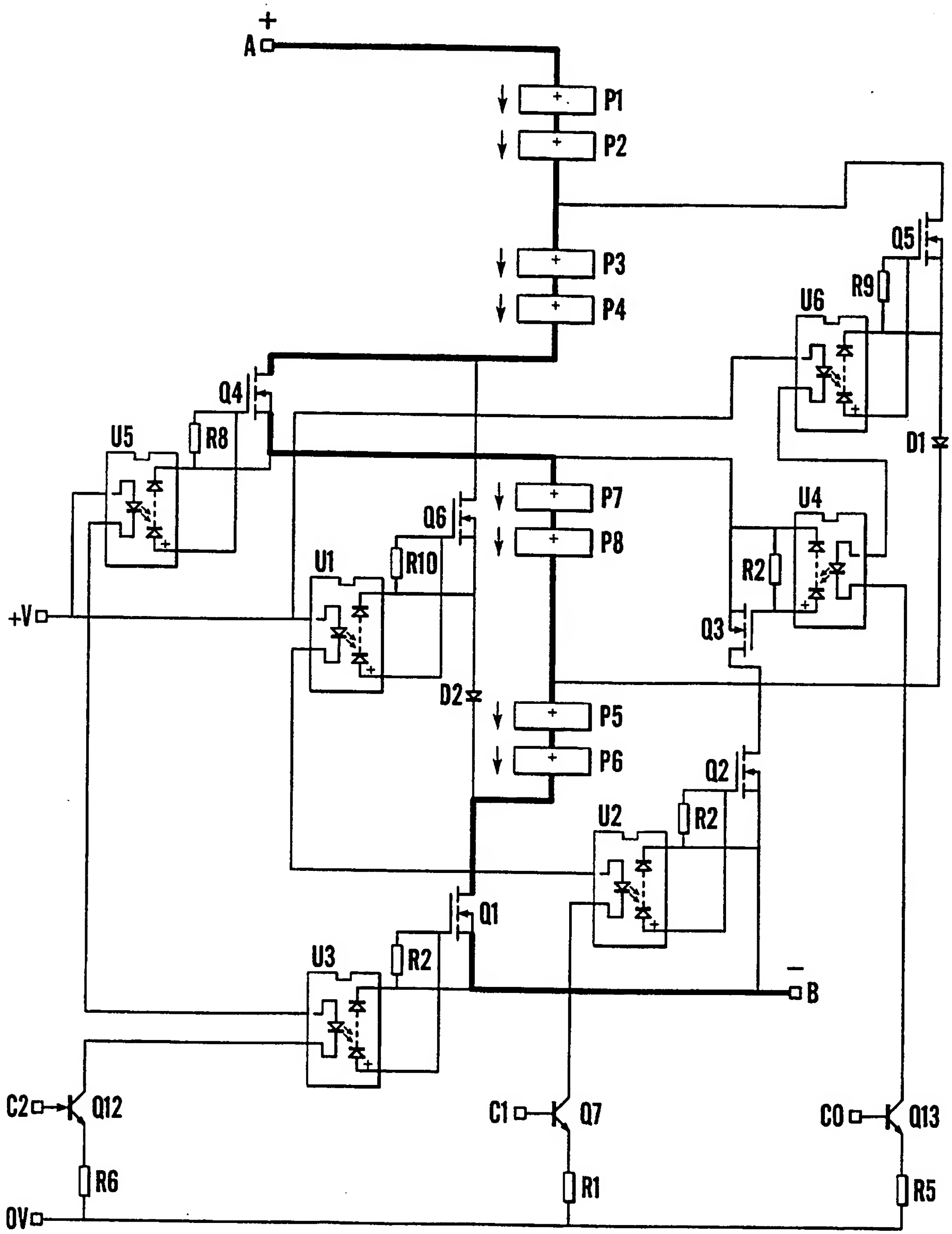

+
A
P1
P2
P3
P4
Q5
R9
U6
D1
Q4
U5
R8
P7
P8
Q6
U4
U1
R10
R2
+V
Q3
D2
P5
P6
Q2
R2
U2
Q1
U3
R2
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.4

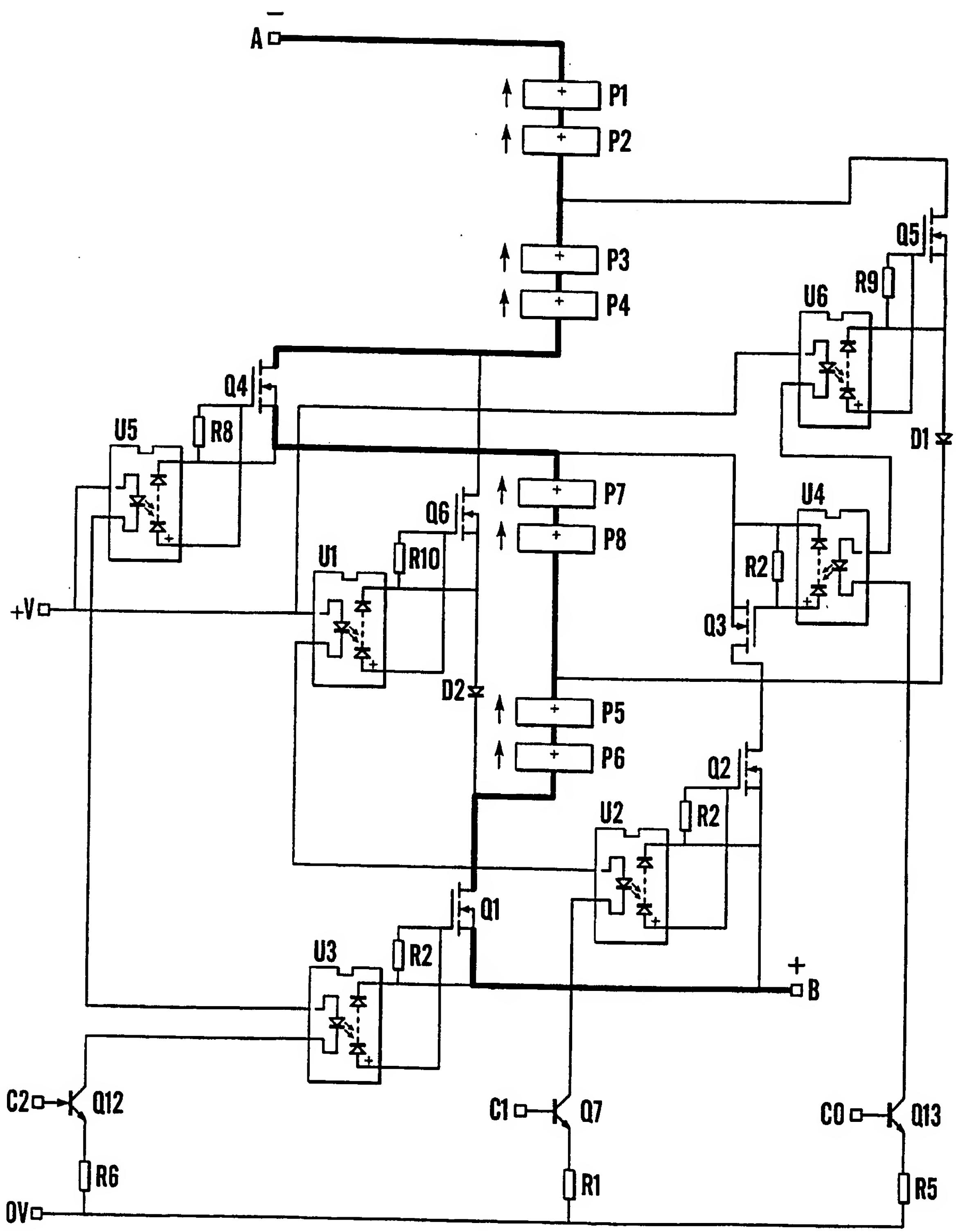

A
P1
P2
P3
P4
Q5
R9
U6
Q4
U5
R8
D1
P7
P8
Q6
U4
U1
R10
R2
+V
Q3
D2
P5
P6
Q2
R2
U2
Q1
U3
R2
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.5

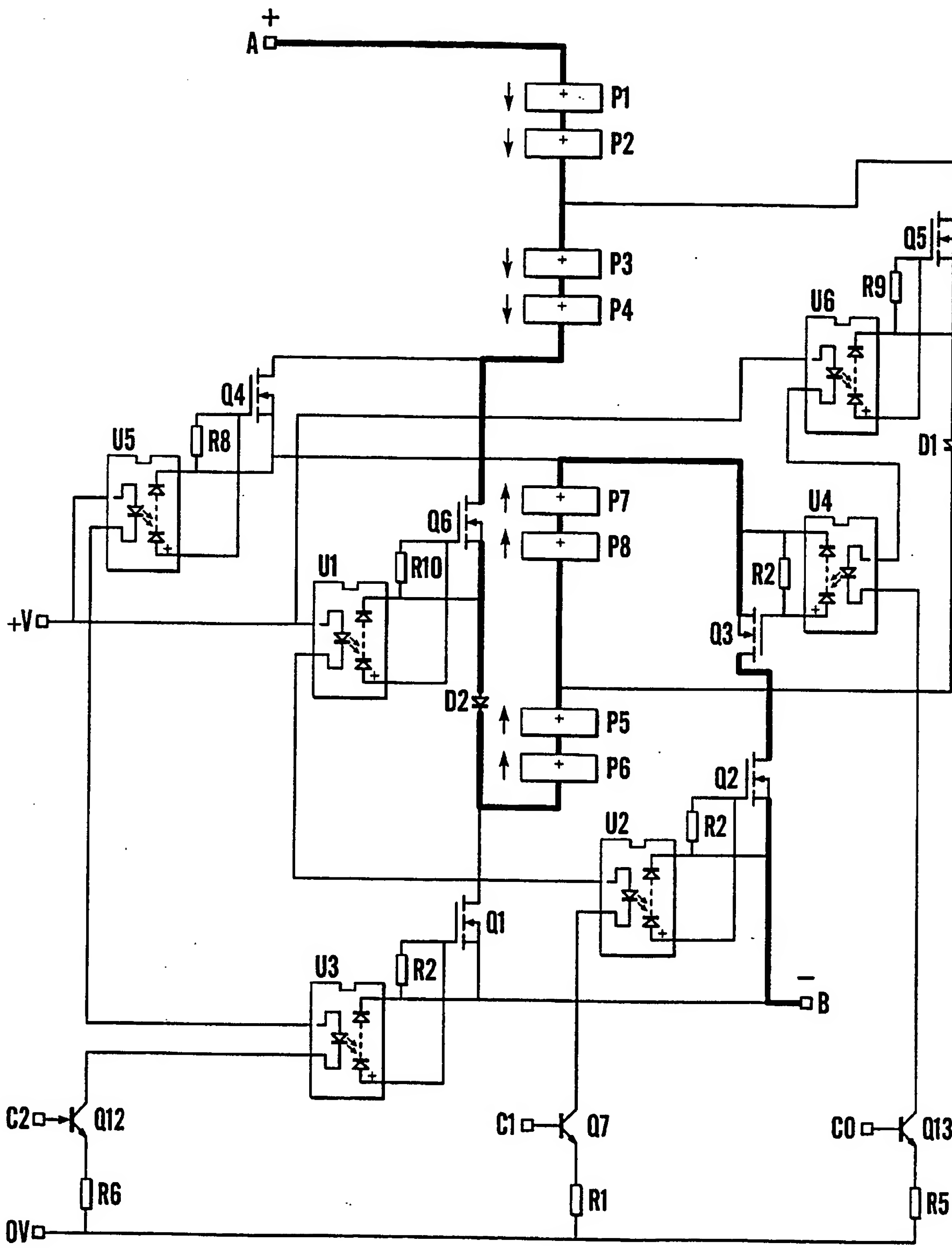

A
+
P1
P2
P3
P4
Q5
R9
U6
Q4
R8
U5
D1
P7
P8
Q6
U1
R10
U4
R2
+V
Q3
D2
P5
P6
Q2
U2
R2
Q1
U3
R2
-
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.6

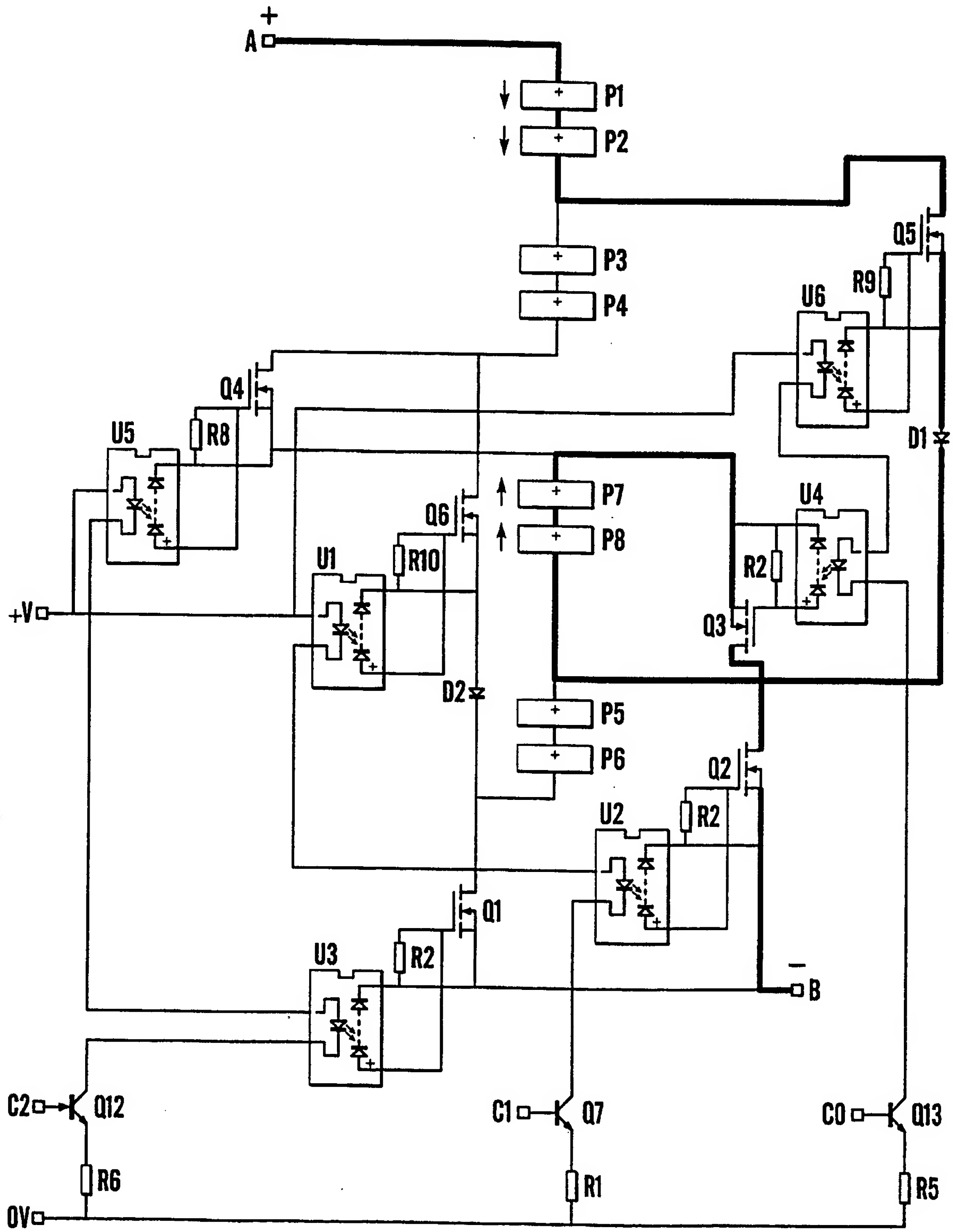

+
A
P1
P2
Q5
P3
P4
R9
U6
Q4
U5
R8
D1
Q6
P7
P8
U4
U1
R10
R2
+V
Q3
D2
P5
P6
Q2
U2
R2
Q1
U3
R2
−
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.7

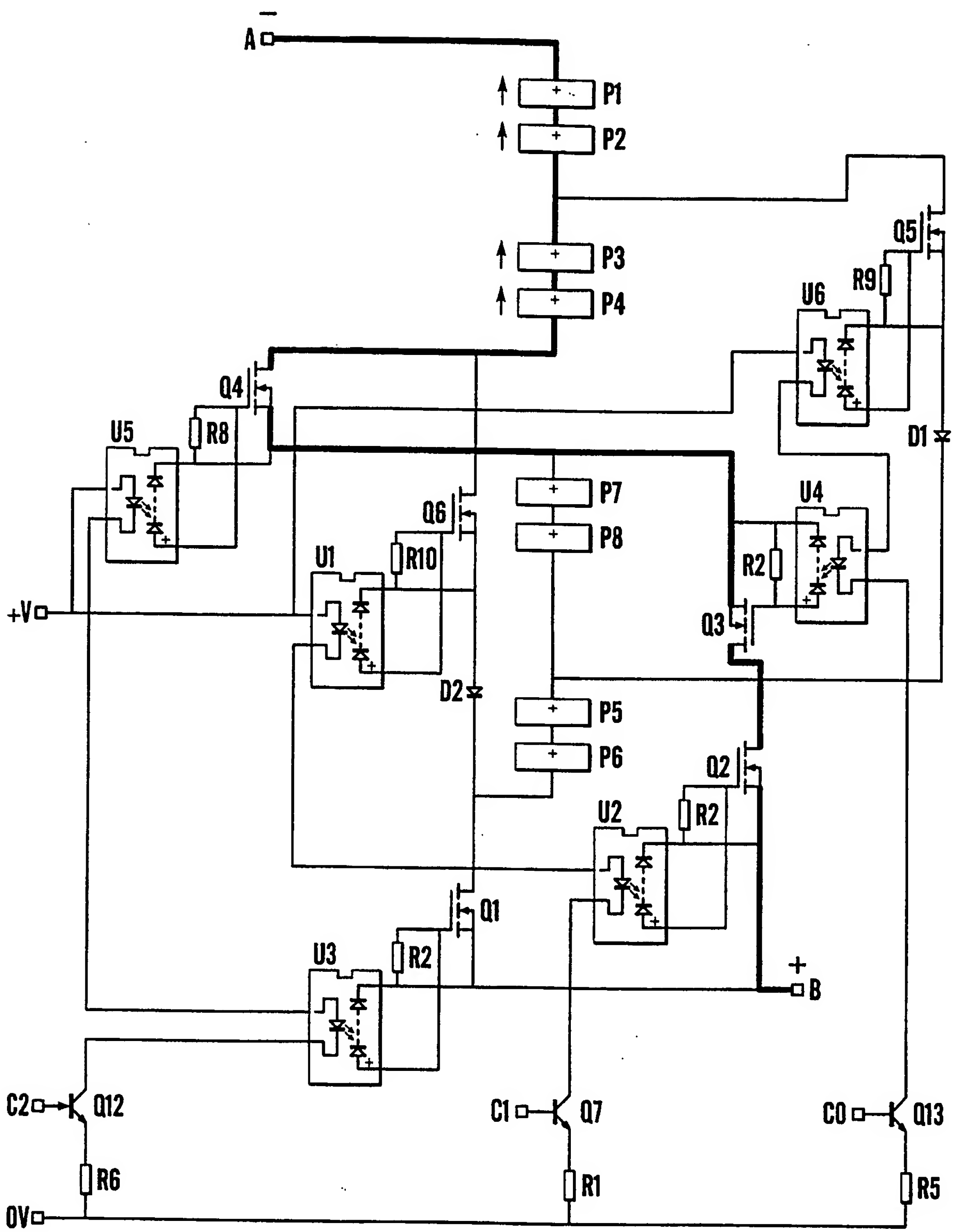

A
P1
P2
P3
P4
Q5
R9
U6
Q4
U5
R8
D1
P7
P8
U4
Q6
U1
R10
R2
+V
Q3
D2
P5
P6
Q2
U2
R2
Q1
U3
R2
+
B
C2
Q12
C1
Q7
C0
Q13
R6
R1
R5
0V

Fig.8

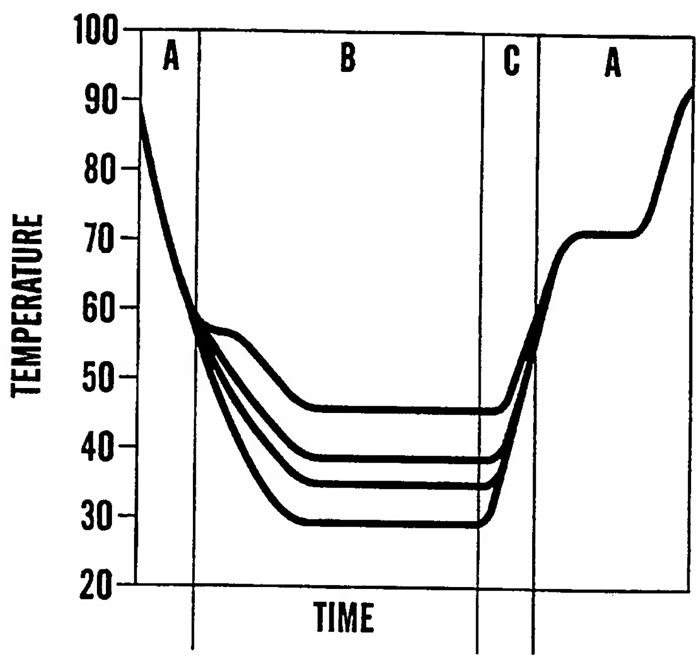


Fig.9

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/03994

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B01L7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 196 46 115 A (EPPENDORF GERAETEBAU NETHELER) 14 May 1998 (1998-05-14) abstract; figures 3-5 column 1, line 26 -column 1, line 55 column 1, line 64 -column 2, line 3 column 2, line 28 -column 2, line 41 column 6, line 23 -column 9, line 24 ---	1-6
A	US 5 525 300 A (DANSSAERT JOHN L ET AL) 11 June 1996 (1996-06-11) abstract; figure 2 column 4, line 64 -column 6, line 55 ---	1-6
A	US 4 679 615 A (LIVNE AVINOAM) 14 July 1987 (1987-07-14) abstract; figures 1-3 column 1, line 35 -column 2, line 17 column 2, line 40 -column 3, line 47 --- -/--	1-6

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2000	25/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Runser, C

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte ‹ional Application No
PCT/GB 99/03994

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 224 536 A (BAUER GUENTER ET AL) 6 July 1993 (1993-07-06) abstract; figures 1,3 column 5, line 42 -column 7, line 13 -----	1-6

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/03994

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 19646115 A	14-05-1998	DE 29623597 U	07-01-1999
		WO 9820975 A	22-05-1998
		EP 0881950 A	09-12-1998
US 5525300 A	11-06-1996	EP 0733098 A	25-09-1996
		JP 9510863 T	04-11-1997
		WO 9511294 A	27-04-1995
		US 5779981 A	14-07-1998
US 4679615 A	14-07-1987	IL 71131 A	30-09-1988
		JP 61149247 A	07-07-1986
US 5224536 A	06-07-1993	DE 8814398 U	16-02-1989
		WO 9005947 A	31-05-1990
		EP 0444144 A	04-09-1991

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: ______________________

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.